

# VIRTUAL COMPUTER VERIFICATION PLATFORM

## ABSTRACT OF THE DISCLOSURE

A virtual computer verification platform is provided with a verifying  
5 and debugging environment so as to develop a new microprocessor chip,  
a new system software, a new firmware and a new peripheral chip.  
The virtual computer verification platform includes a simulation system  
and a set of on-line debugging auxiliary tools, wherein the  
microprocessor chip can be designed in a Behavior model, a RTL model  
10 and a Gate model. The message communication for integrating the  
whole simulation system is implemented through a message passing  
mechanism supported by UNIX IPC (Inter-Process Communication) and  
PLI (Programming Language Interface) supported by Verilog.